Low-loss Silicon Interposer for Three-dimensional System Integration with Embedded Microfluidic Cooling

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Abstract

Novel technology enablers for high-performance three-dimensional (3D) system integration are demonstrated in this paper: (a) A thick silicon interposer with 65 µm diameter and 370 µm tall low-loss polymer-embedded vias on a 150 µm pitch is fabricated and characterized demonstrating a 78% reduction in insertion loss compared to similar-sized conventional TSVs at 50 GHz; (b) Two dice with embedded microfluidic heatsinks and electrical and fluidic microbumps are assembled to an interposer demonstrating lower thermal resistance, chip-to-interposer average electrical microbump resistance of 12.06 mΩ and a robust fluidic microbump interconnection.

Keywords: TSV, silicon interposer, 3D IC and cooling

Introduction

Interconnect performance has emerged as a key bottleneck to achieving high-speed and low-power chip-to-chip communication. To address this challenge, three-dimensional integrated circuits (3D ICs) have been widely explored [1]. Moreover, large-area silicon interposers with dense metallization and through-silicon vias (TSVs) offer high bandwidth-density communication between ICs [2]. Thick silicon is desired for the large-area interposers to ease handling and ensure mechanical stability. However, increasing the interposer thickness increases TSV length and losses necessitating low-loss silicon interposers. Moreover, since the stacking of chips leads to increased thermal resistance and greater power densities, innovative cooling technologies are needed to replace air-cooled heatsinks.

This paper demonstrates the fabrication and characterization of novel technologies to enable high-performance 3D system integration: (a) A 'thick' silicon interposer with 370 µm tall low-loss polymer-embedded vias consisting of copper-filled vias within polymer wells; (b) Assembly of 2 dice with monolithically fabricated back side microfluidic heatsink and electrical and fluidic microbumps to an interposer is also demonstrated. Fig. 1 illustrates an envisioned 3D system with a low-loss silicon interposer supporting 3D IC stacks including embedded microfluidic heatsinks. Microchannels or fluidic vias in the interposer enable coolant transfer to the 3D ICs.

Technology Development and Characterization

A. Polymer-embedded Vias for Low-loss Silicon Interposer

As shown in Fig. 2(a), the fabrication of polymer-embedded vias begins with formation of wells in silicon with a copper seed layer at the base. Next, SU-8 filling and photodefinition [3] are performed to obtain vias followed by electroplating and chemical-mechanical polishing (CMP) to remove overburden copper. Fig. 3 illustrates the fabricated 370 µm tall polymer-embedded vias with 65 µm diameter and 150 µm pitch within a 1.8 mm x 1.8 mm well in silicon.

High-frequency measurements were performed for the fabricated polymer-embedded vias from 100 MHz to 50 GHz, as shown in Fig. 4. A TSV-trace-TSV structure with 400 µm long trace (L chain structure) between the copper vias was measured, matching well to the High-Frequency Structure Simulator (HFSS) results with 3.25 and 0.035 as the relative dielectric constant and loss tangent of SU-8 [4], respectively. The fabricated polymer-embedded vias enable a 78% reduction in insertion loss compared to similar-sized conventional TSVs with 1 µm thick SiO_2 liner and 10 Ω-cm silicon resistivity at 50 GHz (Fig. 4). From the measurements, 0.79 dB insertion loss per GSG polymer-embedded via was obtained at 50 GHz using L-2L de-embedding technique [5] with simulations of 2L chain structure (800 µm long trace).

As shown in Fig. 2(a), redistribution layer (RDL) and fluidic vias can be fabricated in the silicon interposer to transfer a coolant to the assembled ICs as described next.

B. Integration of Novel Chips Over Silicon Interposer

Microfluidic cooling has been widely explored as a potential technology to replace air-cooled heatsinks for 3D ICs [6, 7]. This paper demonstrates, for the first time, the integration of two 1 cm x 1 cm dice with micropin-fin heatsinks, 22,500 electrical microbumps (25 µm diameter on a 50 µm pitch) and 42 fluidic microbumps over a large-area silicon interposer with fluidic vias for coolant delivery to the dice (Fig. 5 and 6).

To fabricate the dice, fluidic vias and micropin-fins are first etched in Si, as shown in Fig. 2(b). Next, a titanium-copper seed layer is deposited over an SiO_2 layer and copper pads are electroplated followed by nickel and solder electroplating over the pads. Lastly, seed layer etching and solder reflow are performed yielding electrical and fluidic microbumps.

Once the microfluidic-cooled chips are fabricated, they are assembled to a silicon interposer using a flip-chip bonder with sub-micron alignment accuracy. Chip-to-interposer electrical connections after the assembly are tested using 4-point resistance measurements and 12.06 mΩ average electrical microbump resistance was measured, as shown in Fig. 7. To ensure a robust sealing by fluidic microbumps, an assembly of the microfluidic-cooled chip and interposer was tested with deionized water pumped continuously for 4 hours at the flow rates of 30 and 50 mL/minute, showing a stable pressure drop and no leakage. Thermal measurements of the microfluidic heat sink demonstrate a normalized thermal resistance of 0.27 $K*cm^2/W$ at 70 mL/minute flow rate.

Conclusion

For high-performance 3D system integration, this paper demonstrates the fabrication and characterization of a thick silicon interposer with low-loss polymer-embedded vias and the assembly of two dice with monolithically integrated microfluidic heat sink and electrical and fluidic I/Os to a silicon interposer.

Acknowledgement

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References

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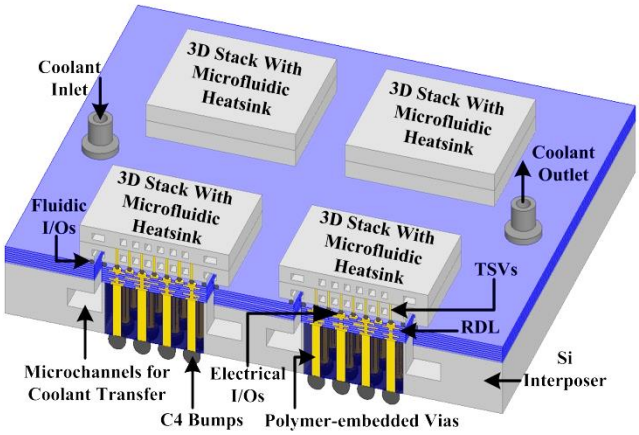

Fig. 1 3D system with a low-loss silicon interposer including microchannels for coolant delivery to 3D ICs with embedded microfluidic heat sinks.

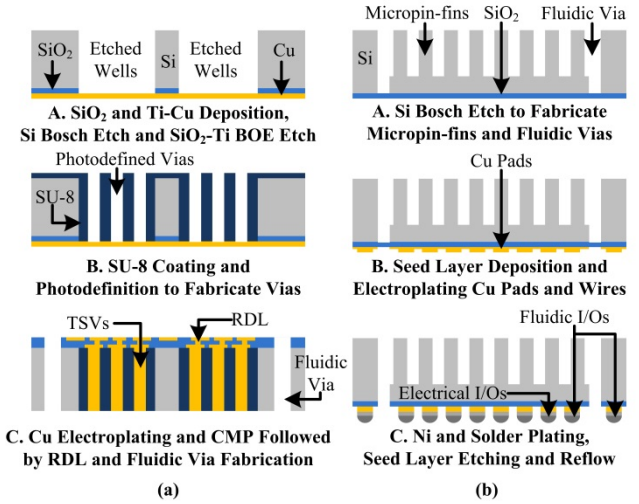

Fig. 2 Fabrication process for (a) low-loss silicon interposer with polymer-embedded vias, RDL and fluidic vias and (b) chip with micropin-fin heatsink and fluidic and electrical I/Os.

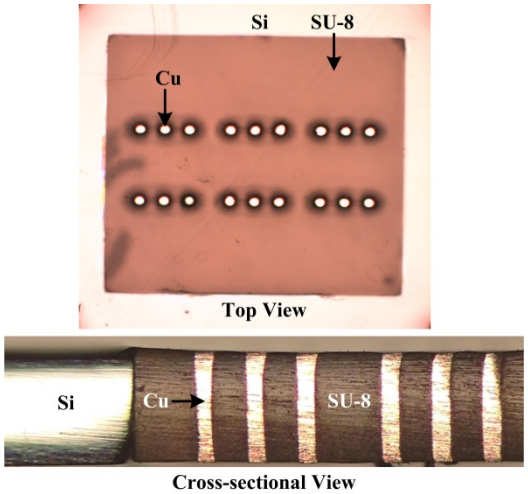

Fig. 3 Fabricated polymer-embedded vias with 65 µm diameter and 150 µm pitch within 1.8 mm x 1.8 mm polymer wells in Si.

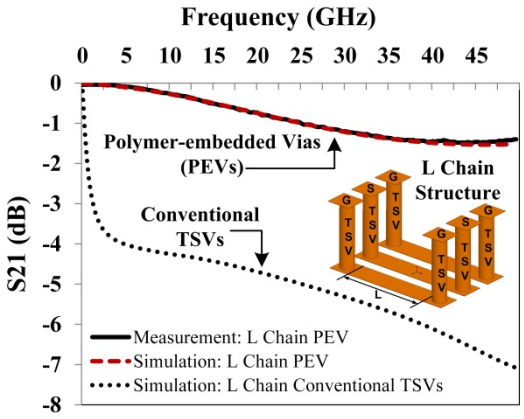

Fig. 4 Polymer-embedded via RF measurement, simulation, and benchmarking with respect to conventional TSVs.

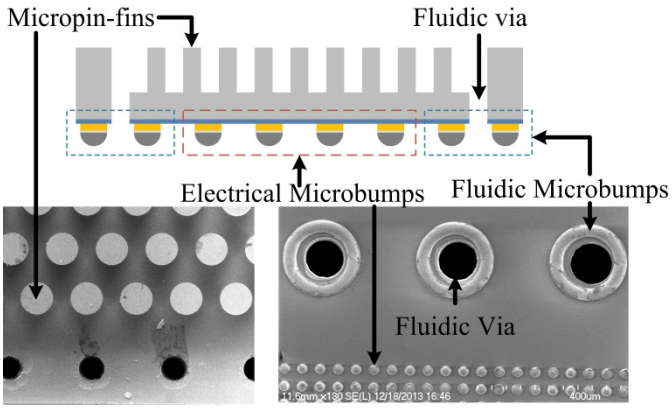

Fig. 5 SEMs of micropin-fins, electrical microbumps, fluidic microbumps and vias.

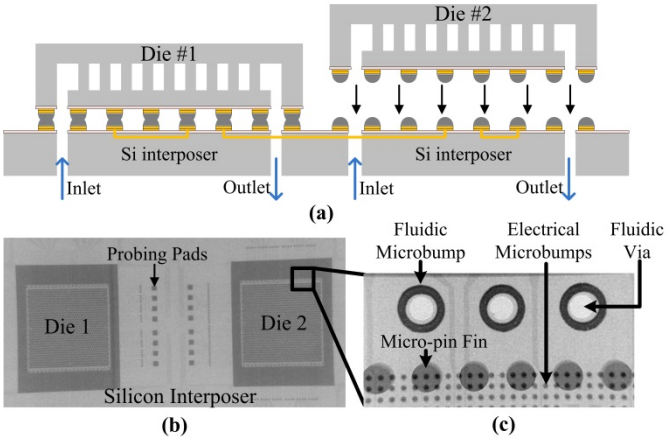

Fig. 6 (a) Flip-chip bonding of two silicon dice with electrical and fluidic microbumps and micropin-fin heat sinks onto a silicon interposer, (b) X-ray image of the bonded sample and (c) Close-up of the bonded electrical and fluidic microbumps and micropin-fins.

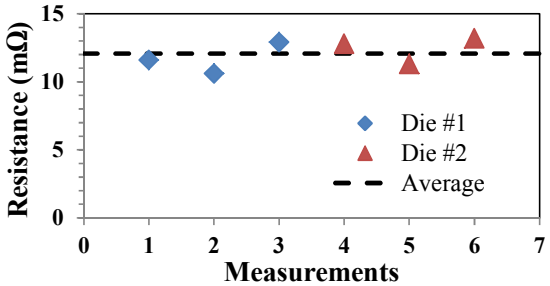

Fig. 7 Four-point resistance measurements of electrical microbumps connecting Die 1 and Die 2 (Fig. 6) to silicon interposer.